IN THE CLAIMS

1. (Currently Amended) A memory array system comprising:

a plurality of memory cells arranged in a data array having a plurality of wordlines traversing the plurality of memory cells, such that a group of the plurality of memory cells is connected to each of the plurality of wordlines; ~~and~~

wordline decoding circuitry for receiving a control signal for activating ~~one of~~ a single wordline ~~and~~ or at least two wordlines ~~of a plurality of wordlines traversing the plurality of memory cells~~ during a data array accessing cycle; and

means for interchanging between a single-cell array and a twin-cell array mode of operation of a set of the memory cells connected to the activated wordline.

2. (Original) The memory array system according to Claim 1, wherein said wordline decoding circuitry includes a pre-decoder circuit having a logic circuit for receiving the control signal and two logic inputs and outputting at least one wordline selection signal to wordline activating means.

3. (Original) The memory array system according to Claim 2, wherein said logic circuit includes two pairs of transmission gates and first and second NAND logic gates coupled to a respective pair of the two pairs of transmission gates, wherein each pair of transmission gates receives the control signal, one of the two logic inputs, and an inverse input of one of the two logic inputs.

4. (Original) The memory array system according to Claim 2, wherein said wordline activating means includes a first and a second line shifter and a wordline driver circuit having wordline drivers for activating a respective one of the plurality of wordlines.

5. (Currently Amended) The memory array system according to Claim 1, wherein said wordline decoding circuitry includes the means for interchanging ~~at least a group of~~ between the single-cell array and the twin-cell array modes of operation of the set ~~plurality of~~ memory cells ~~coupled to at least one activated wordline between single-cell and twin-cell array operation~~.

6. (Currently Amended) The memory array system according to Claim ~~5~~ 1, wherein in said single-cell array mode of operation data is stored in a single-cell array format and in said twin-cell array mode of operation data is stored in a twin-cell array format.

7. (Original) The memory array system according to Claim 1, wherein said plurality of wordlines have an interleaved arrangement, wherein a group of wordlines of the plurality of wordlines are activated from a left side of the data array and a group of wordlines of the plurality of wordlines are activated from a right side of the data array.

8. (Currently Amended) The memory array system according to Claim 1, further comprising an address directory register for storing the address of each memory cell

operating in a single-cell array mode of operation and the address of each memory cell operating in a twin-cell array mode of operation.

9. (Original) The memory array system according to Claim 1, wherein the memory cells are selected from the group consisting of DRAM and TRAM cells.

10. (Currently Amended) A memory array system comprising:

a plurality of memory cells arranged in an array having a plurality of wordlines traversing the plurality of memory cells; ~~, and~~

a memory controller having means for accessing an address directory register storing an address and a status of each of the plurality of memory cells, said memory controller further having means for determining the address and status of at least one of the plurality of memory cells and means for activating ~~one of~~ a single wordline ~~and~~ or at least two wordlines ~~of a plurality of wordlines traversing the plurality of memory cells~~ during a data array accessing cycle; and

means for interchanging cells between a single-cell array and a twin-cell array mode of operation of at least one of the plurality of memory cells.

11. (Original) The memory array system according to Claim 10, wherein said memory controller further comprises means for updating the status of the at least one of the plurality of memory cells.

12. (Currently Amended) The memory array system according to Claim 10, ~~further comprising means for interchanging at least one of the plurality of memory cells between single-cell and twin-cell array operation,~~

wherein in said single-cell array mode of operation data is stored in a single-cell array format and in said twin-cell array mode of operation data is stored in a twin-cell array format.

13. (Original) The memory array system according to Claim 10, wherein the memory cells are selected from the group consisting of DRAM and TRAM cells.

14. (Currently Amended) Wordline decoding circuitry for controlling ~~dual~~ wordline activation for a memory array having a plurality of memory cells, said wordline decoding circuitry comprising:

circuitry for receiving at least one control signal; ~~and~~

wordline activation circuitry for enabling single wordline activation or dual wordline activation according to said received at least one control signal; and

circuitry for interchanging between a single-cell and a twin-cell array mode of operation of at least one memory cell.

15. (Currently Amended) Wordline decoding circuitry according to Claim 14, wherein said wordline activation circuitry includes the circuitry for interchanging between the single-cell array and the twin-cell array mode of operation of the at least one

~~of a plurality of~~ memory cells ~~of the memory array between single-cell and twin-cell array operation~~,

and wherein in said single-cell array mode of operation data is stored in a single-cell array format and in said twin-cell array mode of operation data is stored in a twin-cell array format.

16. (Currently Amended) ~~The memory array system~~ Wordline decoding circuitry according to Claim ~~15~~ 14, wherein the at least one memory cells ~~are~~ is selected from the group consisting of DRAM and TRAM cells.

17-20. (Previously Canceled)